 



University of Bahrain

College of Information Technology

Department of Computer Engineering

Background pattern

Description automatically generated

Heart Analysis

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# Objectives

* Implement Heart Analysis Algorithm
* Make an GUI for the Analysis
* Learn how you can use Signal

# 1.Introduction :

We have chosen to do MIPS pipelined process because it’s something that we saw at the beginning of the course and have heard about it from other majors and other university like ETH Zuirch from Professor Onur Multlu’s Lectures that are available in YouTube for free and also we were inspired to do it since the book Digital Design and Computer Architecture by David Money Haris and Sarah L.Harris which really a good reference for many course that we took ITCE112/250 and ITCE211/251 and finally this course so we felt that would be a good opportunity to use the material available in this book one more time for the project where in chapter 7 they explained clearly how you could design MIPS pipelined processer and we follow the same approach of the book were we will explain each component first then will connect all the ideas together .

# 2. Tools

## 2.1Quartus lite prime 20.1

We mainly used Quartus to synthesis our code and use it’s RTL viewer to get clear idea of how the component are connected

## 2.2MODELSIM Altera

To do our simulation and check the validity of the code

## 2.3Vscode

We use it as code editor since have very useful extension that help you code and many shortcuts that let you work much faster and efficiently and some it’s have some AI that suggest code biased on your style of coding

## 2.4TensorHDL

This an extension in vscode we want mention because it’s help us generate all the tables that will be in the report and it’s a tool that is used by professionals to document and simulate there codes but due to the limitation of Quartus lite prime we could not use it’s full potential